Supply tube - electrical
Budapest contribution

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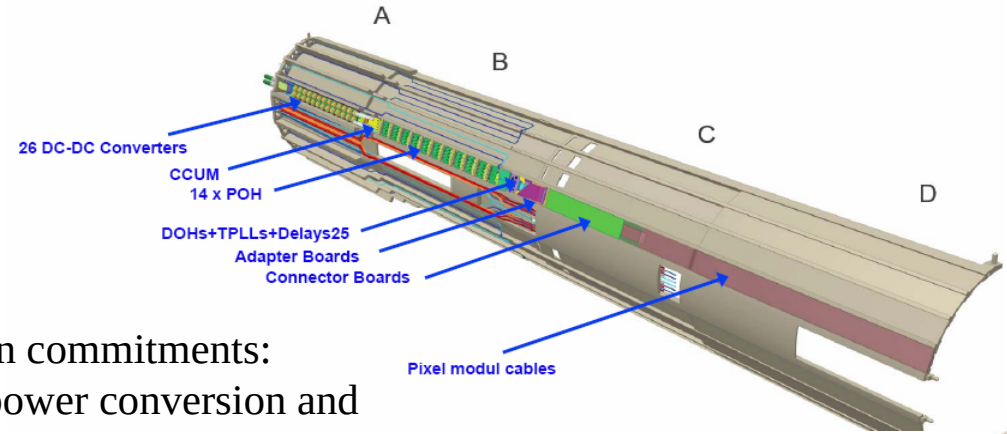
Wigner Research Centre for Physics

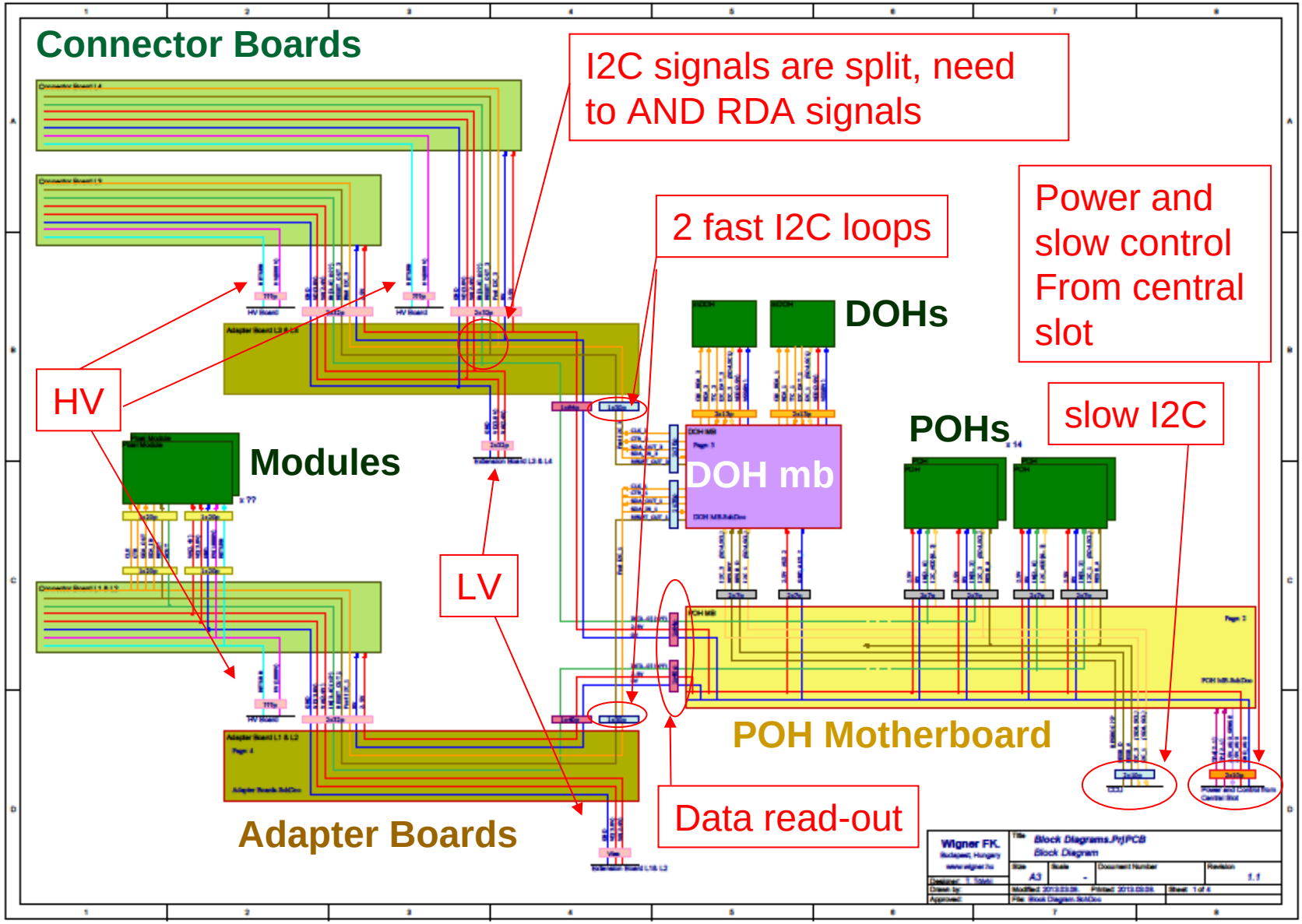
Engineering Design and Electronics System Review of the Phase I Upgrade Pixel Detector, Friday, 6 December 2013

Overview



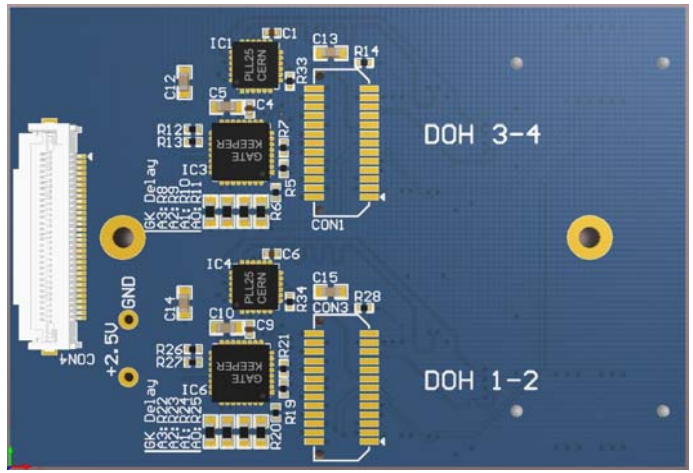
- Aachen commitments:
  - power conversion and distribution boards in **Section A/B**
  - slow I2C control for the supply tube
- Budapest commitments:
  - power distribution in **Section C**
  - fast I2C control for the ROCs
  - data-readout

Block diagram of Section B and C

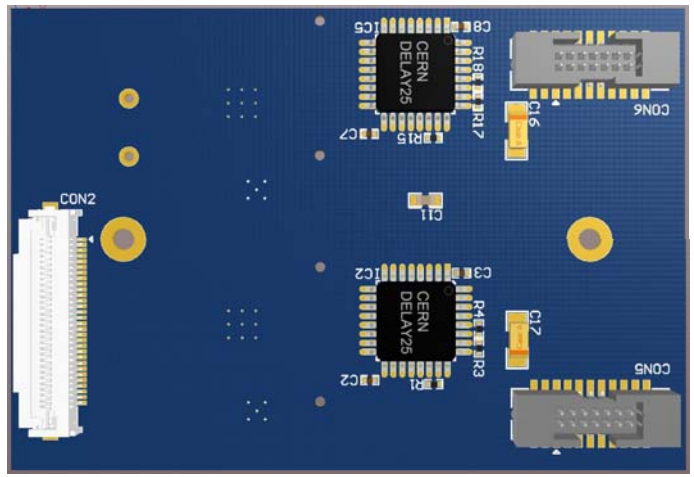


DOH motherboard – detector control

- Purpose:
  - Timing of master clock for read-out groups
  - Decoding trigger signals
  - „fast” I2C protocoll for programming module TBM and ROC registers (DAC)
- Receives from POH motherboard
  - auxiliary power and ground
  - „slow” I2C programming signals
- Two independent „fast” I2C loop for Layer 1&2 and Layer 3&4
  - Hosts two DOH-s on the top connected to the „pixel” FEC-s
  - Key, active components for each loop:
    - Tracker PLL (trigger decoding),
    - Delay25 (I2C delays and clock timing),
    - GateKeeper chips
  - I2C addresses are „hard-wired”
- Status: minimizing PCB length to maximize room for POH pitch, nearly ready for prototpye production



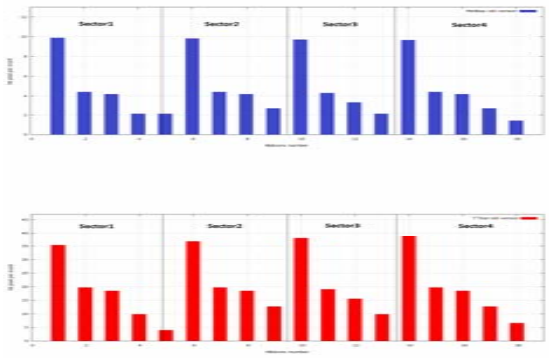
Top side of DOH motherboard



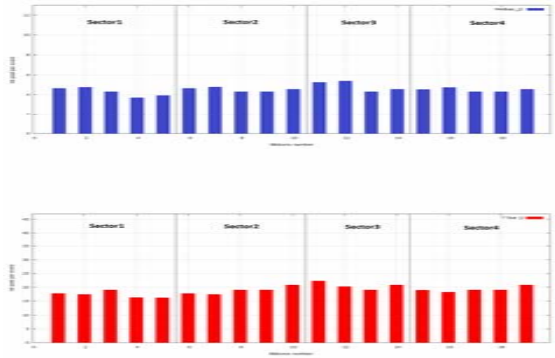
Bottom side

POH motherboard – data read-out

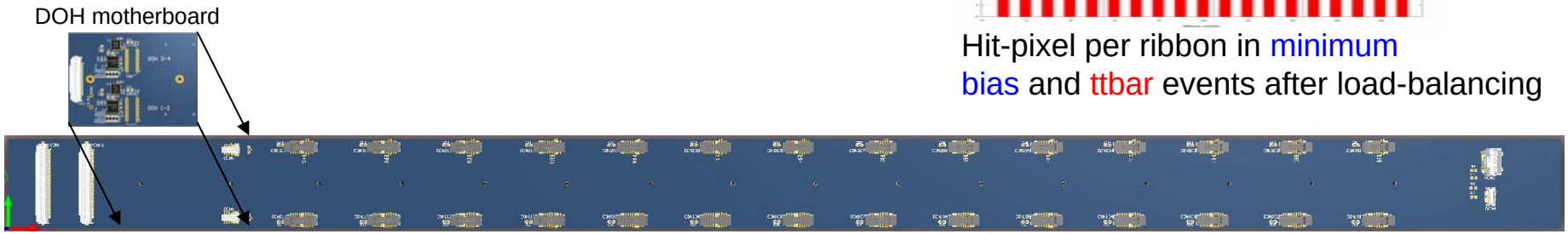
- Purpose:
  - Digital signal conversion to optical links by top mounted POH-s
  - Distributes auxiliary power and „slow” I2C to DOH motherboard, POH-s, and Connector Boards
  - Hosts temperature sensors
- Auxiliary power is recieved from central slot
- „slow” I2C received from CCU board
  - POH I2C addresses are „hard-wired” at the connectors
- 14 POH-s are seated on top
  - 7-7 POHs permanently assigned for Layer 1&2 and Layer 3&4 (not all used in every sector)
  - Data signal routing facilitates load balancing per optical fiber ribbon (12 fibers)
- Status: PCB layout desing is ongoing based on final decision on POH spacing



Hit-pixel per ribbon in minimum bias and ttbar events before load balancing

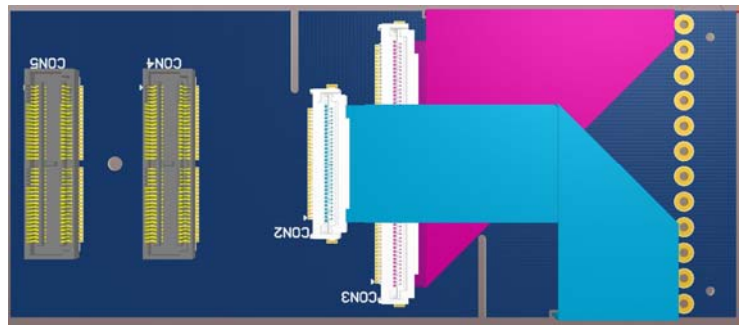


Hit-pixel per ribbon in minimum bias and ttbar events after load-balancing

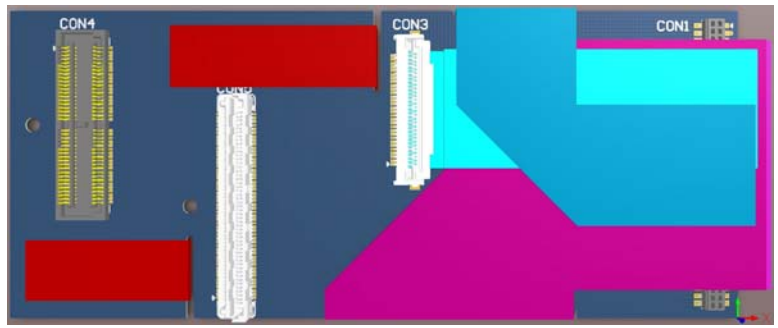


Adapter boards – signal merging

- Purpose: hosts connectors in order to **merge**
  - „fast" I2C signals (from DOH motherboard),
  - LV for ROCs (from Extension boards)
  - Data signal routed to the POH motherboard
- Two independent boards for Layer 1&2 and Layer 3&4
  - RDA of the „fast" I2C signal needs to be AND-ed
- Sends auxiliary power to LCDS chips driving signals on the module cables
  - Auxiliary power received from POH motherboard
- Kapton (polyimid) dielectric layers in order to minimize thickness
  - Better HV isolation
  - Less rigidity even with FR4 in one layer
- Status:
  - Parameters are defined, close to ready for prototyping



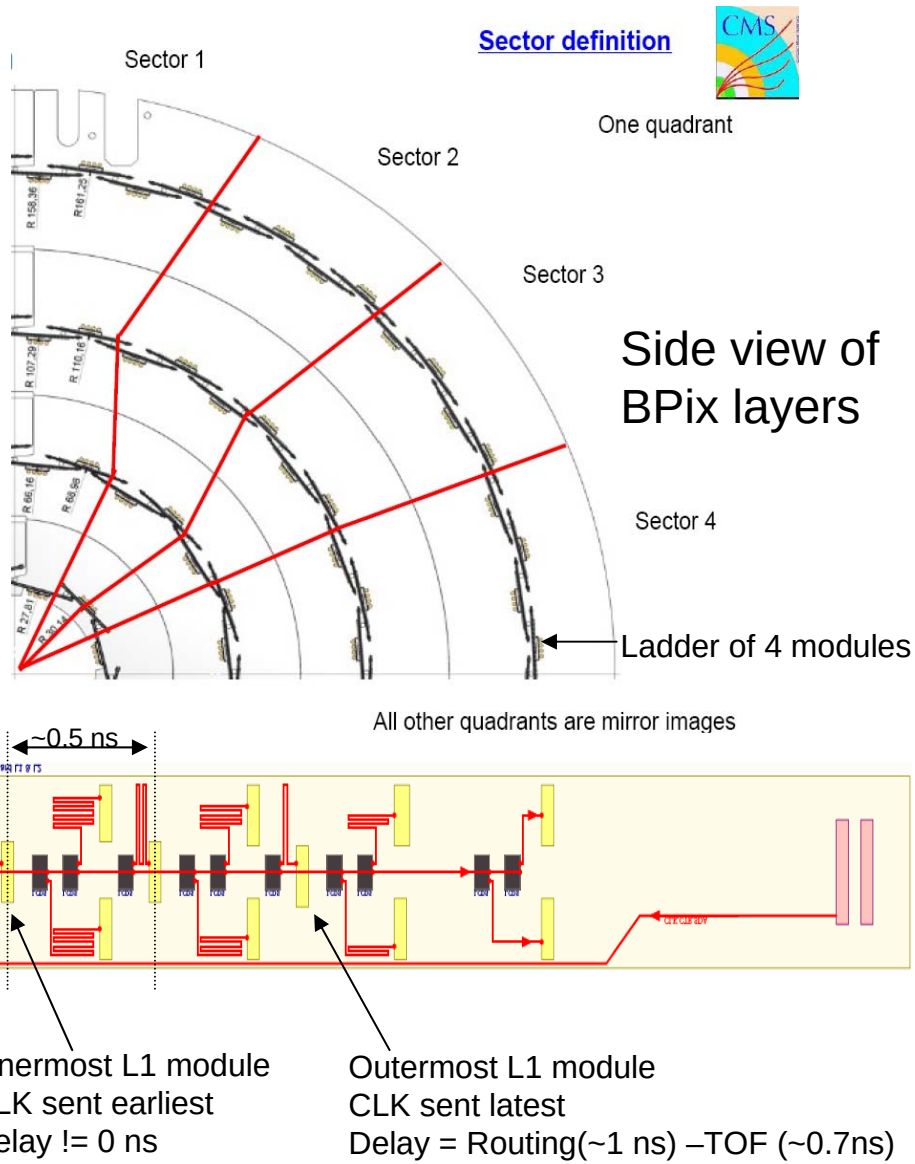
Adapter board for Layer 1&2



Adapter board for Layer 3&4

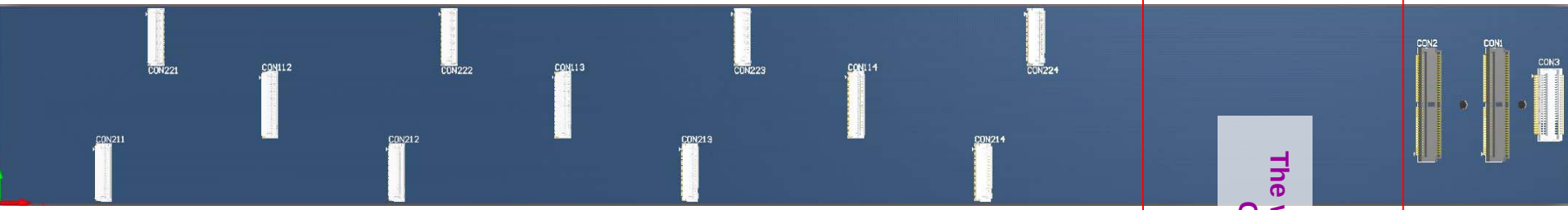
Connector Boards – module connectors

- Purpose:
  - Hosts connectors for module cables and LCDS driver chips
  - Connector positioning facilitates sector definitions
  - Time-alignment of modules
- Connector positioning is a challenge due to ladders on Layer 1-3 not being multiples of the number of sectors (4)
- Module timing
  - Accuracy of ~0.5 ns
  - All modules within a read-out group aligned by Delay25 (on DOH motherboard)
  - Individual modules
    - Corrected for module cable length
    - Corrected for time-of-flight
  - Two possible solutions
    - LCDS chip wiring
    - Meandering of CLK/TRG/SDA on PCB

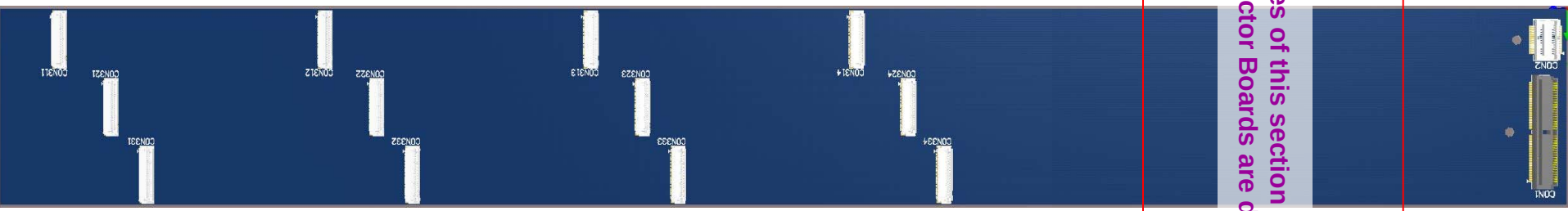


Connector Boards – connector positioning schematics

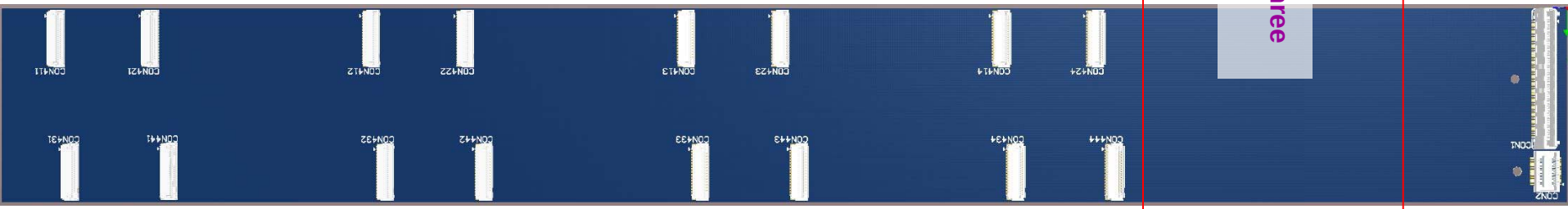
Connector Board L1&L2, Components Side (Top View)



Connector Board L3, Components Side (Bottom View)



Connector Board L4, Components Side (Bottom View)



The widthes of this section of the three Connector Boards are different

Pictures are for illustration only, Connector Board lengthes are different.

Quality assurance

Time schedule and manpower

Summary

- Boards mechanical specifications are defined
- Block diagrams and schematics have been drawn
  - More details at http://www.rmki.kfki.hu/~tivadar/CMS_BPIX_SupplyTube
  - Pin-out of some signal connectors are not yet finalized
- In the process of designing PCB layouts
  - Trial routing on critical PCB-s have been performed
  - Final routing of connector boards need to wait for
    - final decision on module cable length from prototype structure,
    - and subsequent finalization of module timing scheme
- Prototyping a single sector is forseen in Q1 of 2014

Backup

Cost estimate

Board	Type	Sector	# per slot	# total	# incl. spares	Responsible institute	Cost estimate [kSFr] Euro x 1.2
POH motherboard		B	1	32	40	Budapest	**15**
DOH motherboard		C	1	32	40	Budapest	**6**
Adapter board	L 1&2	C	1	32	40	Budapest	**5**
	L 3&4	C	1	32	40	Budapest	**6**
Connector board	L 1&2 S1	C	1	32	40	Budapest	**7 → 10..12**
	L 1&2 S2	C					**10..12**
	L 1&2 S3	C					**10..12**
	L 1&2 S4	C					**10..12**
	L 3	C	1	32	40	Budapest	**7**
	L 4	C	1	32	40	Budapest	**7**