CMS Trigger Short Term Upgrade Plans and Technology Background

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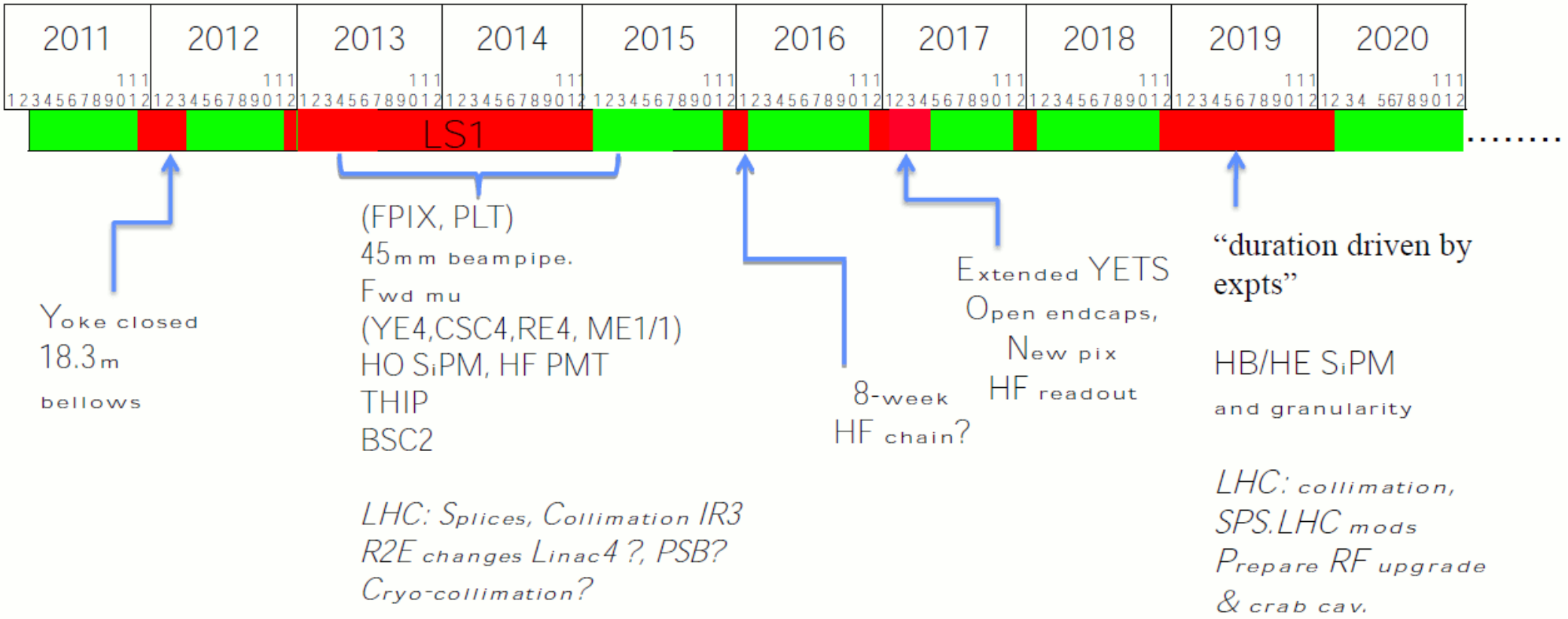
LHC Schedule – CMS preference



CMS Upgrade outline

- Two Upgrade Phases
  - aligned with Long Shutdowns
  - uncertain as LHC planning is
- Phase 1
  - 2013
    - Narrower Beampipe
    - New detector layers
      - CSC
      - RPC
  - 2016
    - New Pixel Detector: 4 layers, lower mass
    - Calorimeter Trigger
- Phase 2
  - Probably 2020 or later

LHC features

- 2013-2014
  - Linac4 commissioning
    - with 25ns beam hard to go beyond the present levels
    - with 50ns beam expect double intensity
    - probably mixed 25ns – 50ns Runs (but much less 25ns)
  - increase to 4TeV
- 2016
  - 6,5TeV (?)

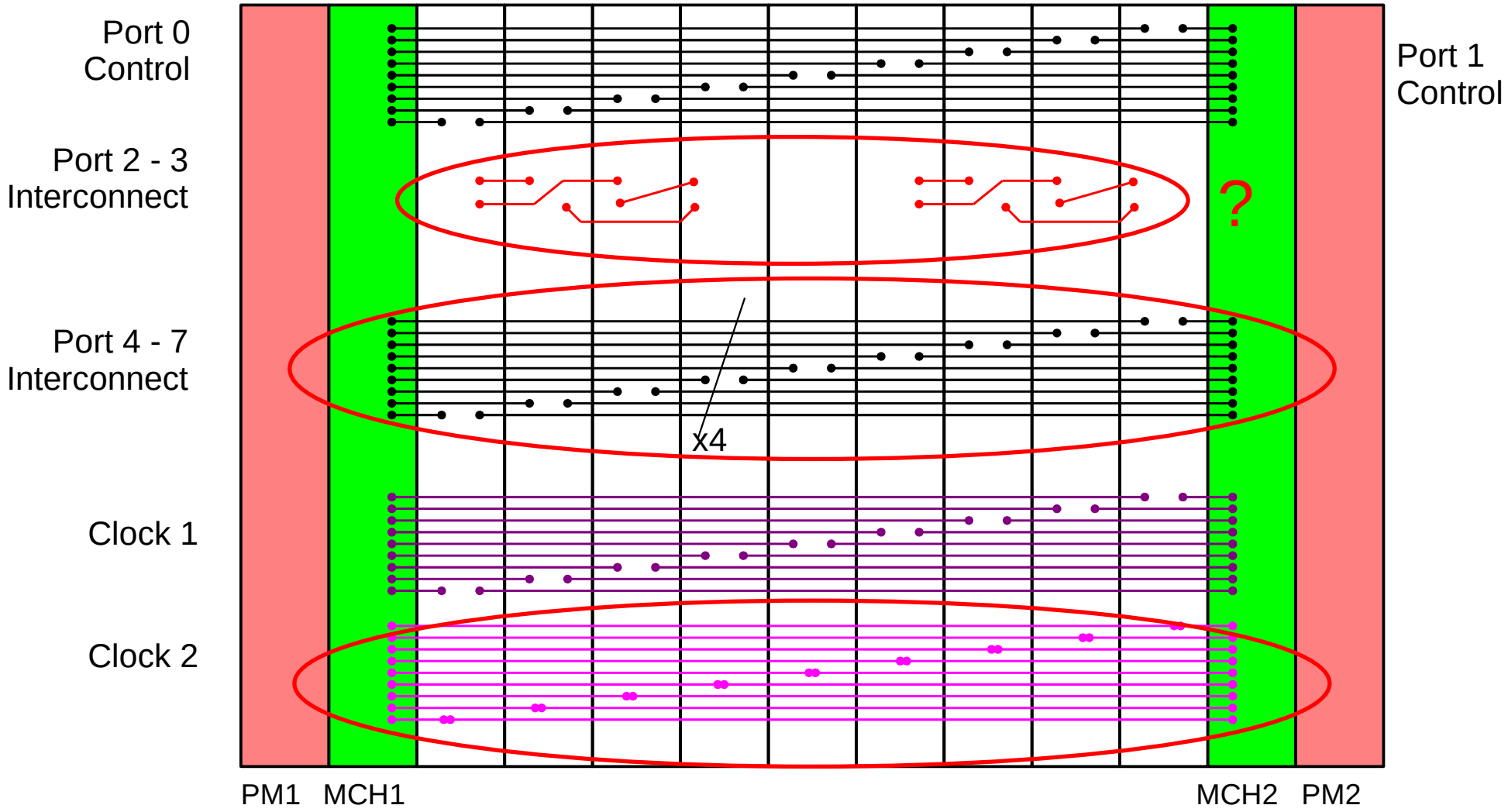
Trigger Upgrade

- “Physics driven design” - few very good arguments
  - Almost sure: pileup increases
    - needs improved resolution
    - improved purity
  - Cross trigger features
    - already built in into GT
    - better exploit combinations
  - Better quality handling
    - important when combining Trigger Objects
- Technology Background
  - maintenance problems everywhere
  - for new developments VME obsolete
    - decreasing support
    - data bandwidth problems
      - for experiments downloading big LUTs
      - for experiments with on-line spy usage
  - GT handles 128 Trigger Menus – starts to be unsufficient

µTCA Platform

- Emerging telecommunications standard
  - important features for high reliable service
    - standardized power management
    - standardized cooling
    - standardized “slow control”
    - high level of redundancy – probably not needed for Trigger applications
      - hot plugging
      - double PS and Control
  - high speed serial links (“Fat Pipes”) on the Backplane
    - up to 6.5 or 10 Gbps
      - in real life max. 3.5Gbps
    - good fit for Trigger Data distribution
    - question is the effect of the serialization – deserialization on the Latency
  - small size
    - probably extensive use of the biggest Board size: 180x148mm
    - a standard extension in preparation allowing backside connection
  - control over Gbit Ethernet

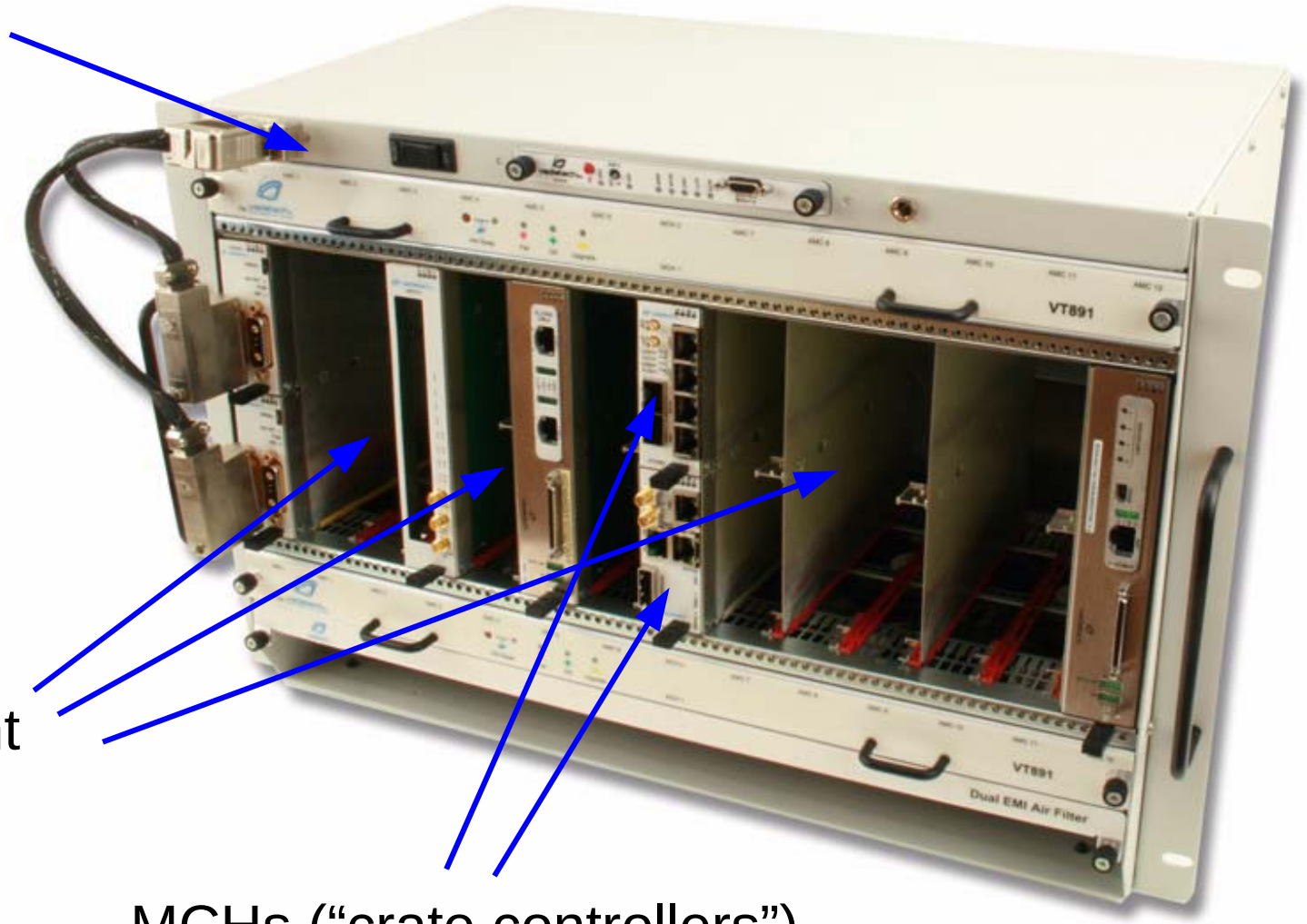
µTCA – a Solution



Two Power Modules, two MCH (controllers) for redundancy

Vadatech VT891 µTCA Crate
possible candidate

Power Supply

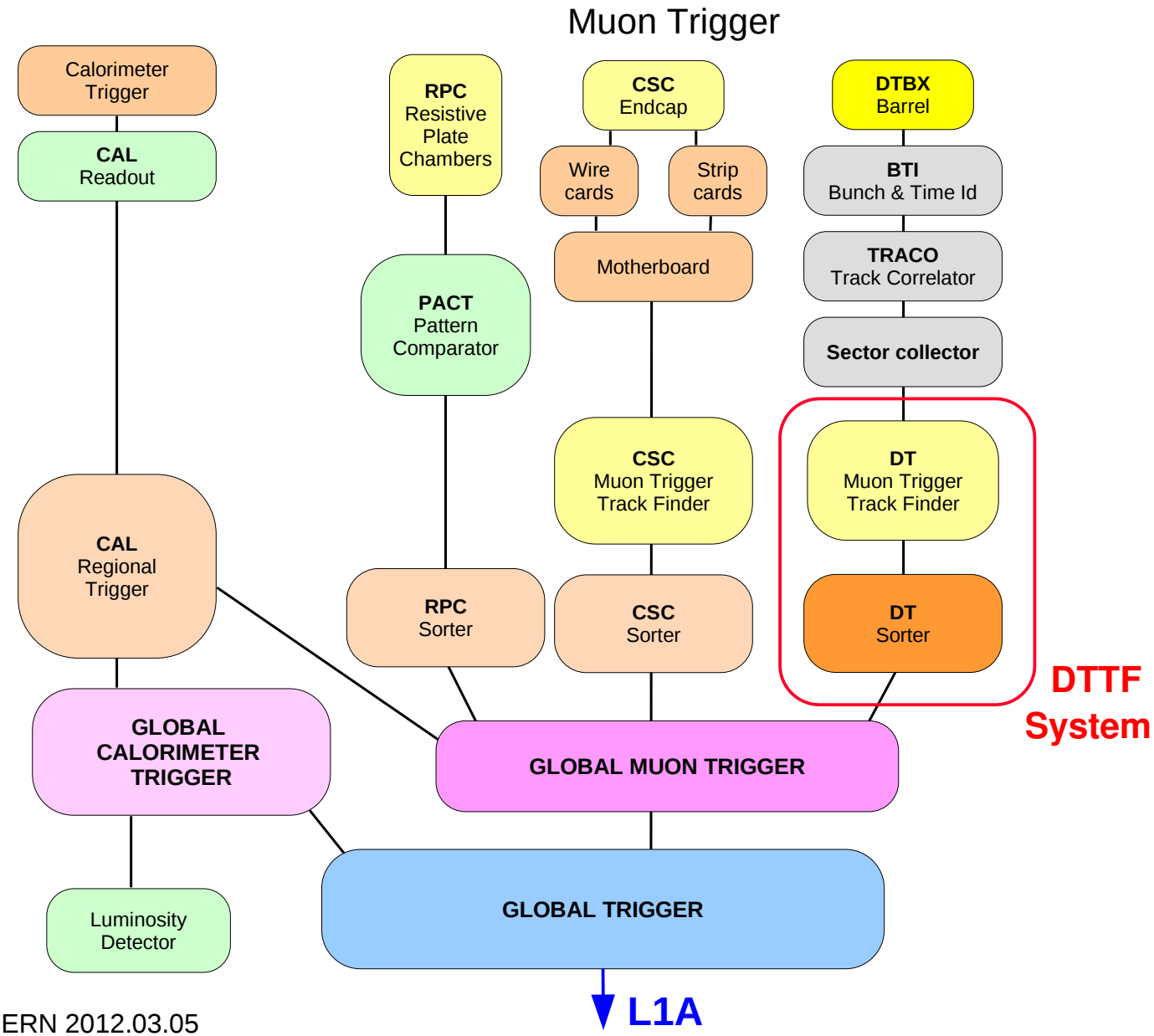


12 Slots for
double height
double width
ACMs

MCHs (“crate controllers”)

CMS Trigger Basics

CMS First Level Trigger Chain



Calorimeter Trigger Plans

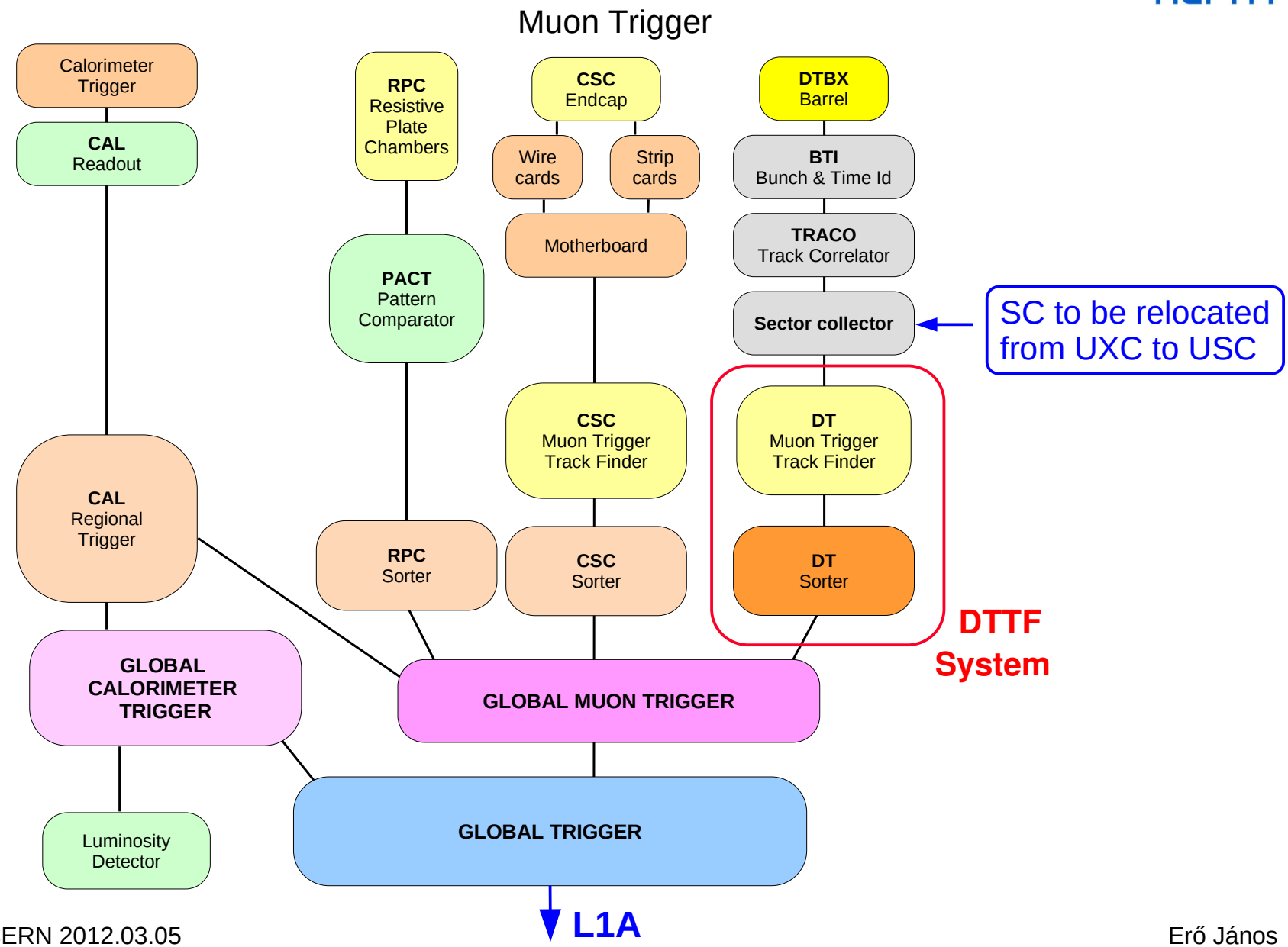
- Calorimeter Trigger always in change
  - Trigger Output changed already twice
- Physics case: new clustering scheme
  - simulated in higher pileup scenarios
- Two designs
  - traditional pipelined architecture
    - well understood technology
    - simpler routing
    - fixed latency
  - “time-multiplex” design
    - avoids pre-clustering
    - allows more complex algorithms
    - less data exchange
    - easier scalability
- Probably the traditional design wins

TTC System Upgrade

- Present TTC performing well
  - Tasks separated between Global Trigger and TTC system
  - Partitioning not fully supported on TTC level
    - in addition GT and DAQ partitioning are different
- Merging with GT or some of its functions
  - question: level of merged functions
  - boundary between these systems
- New idea: use Passive Optical Network (PON) technology
  - Telecom networking practice
    - downstream: broadcast network
    - upstream: channel arbitration
    - no active elements between endpoints
  - structure very similar to CMS TTC sytem
  - commercial components already available, more common in the future

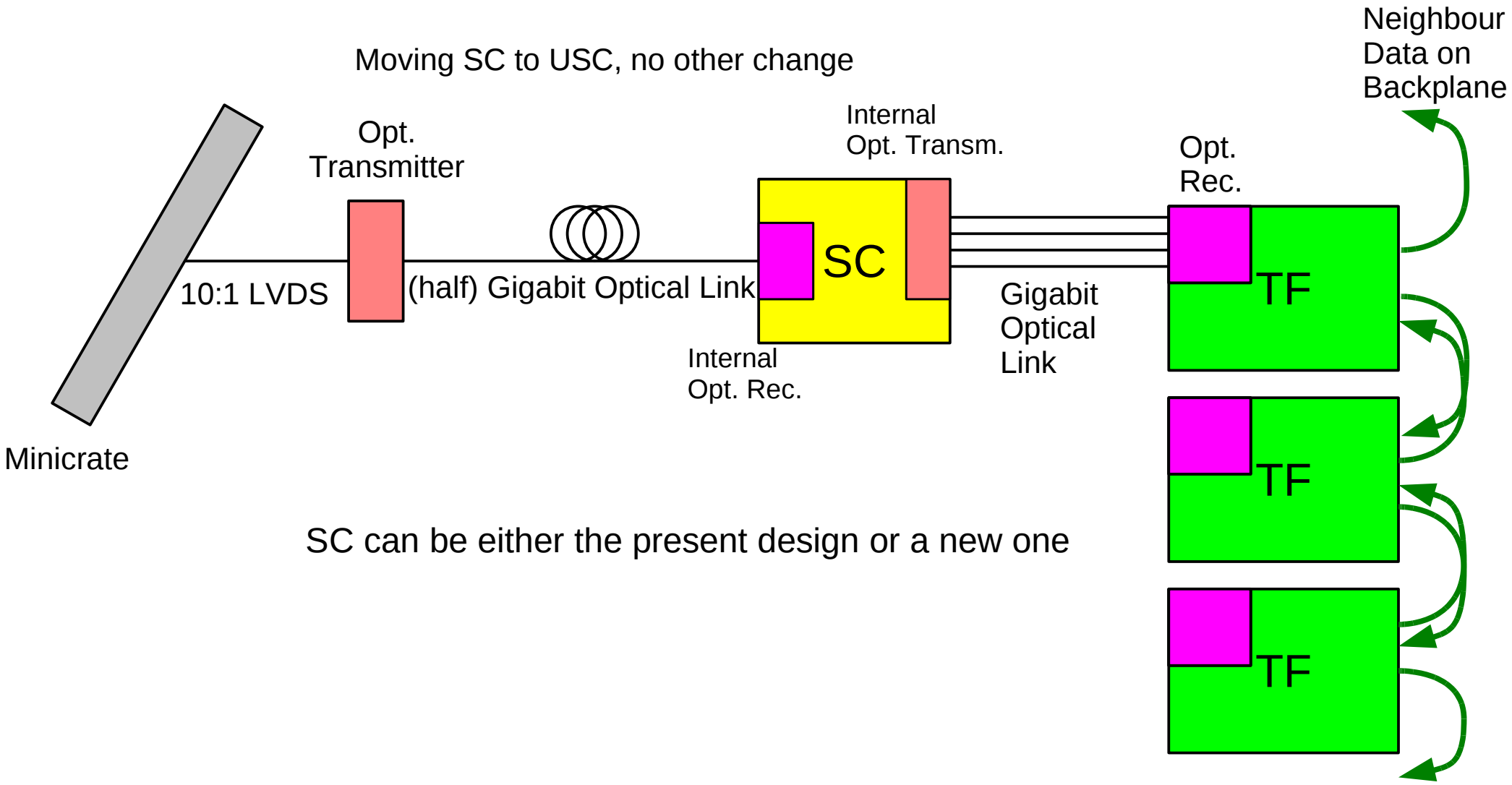
CMS Trigger Basics

CMS First Level Trigger Chain



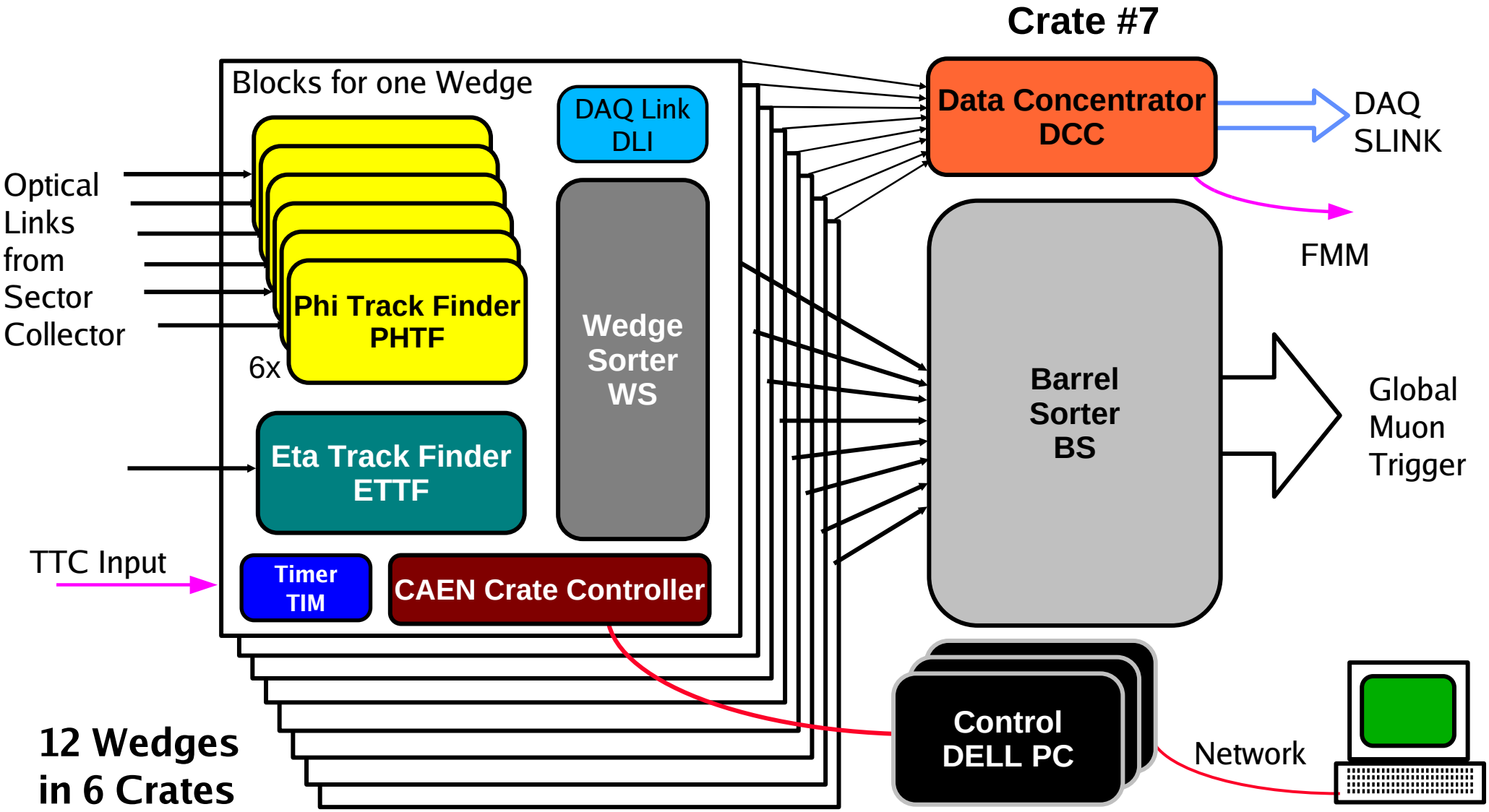
SC to USC and DTTF solution

(shown Trigger Chain only)



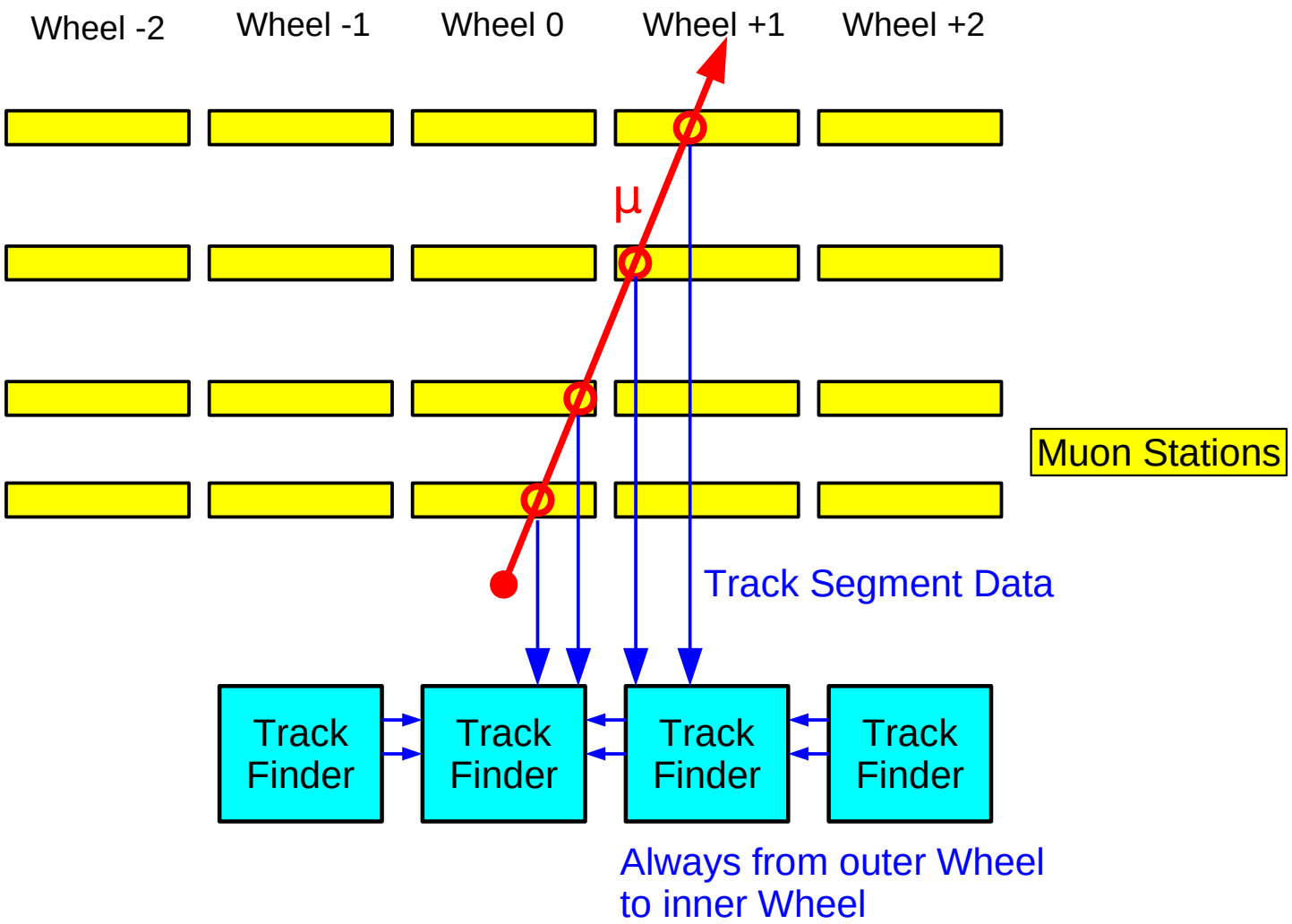
Present DTTF Structure

Sector based



Neighbour Connections

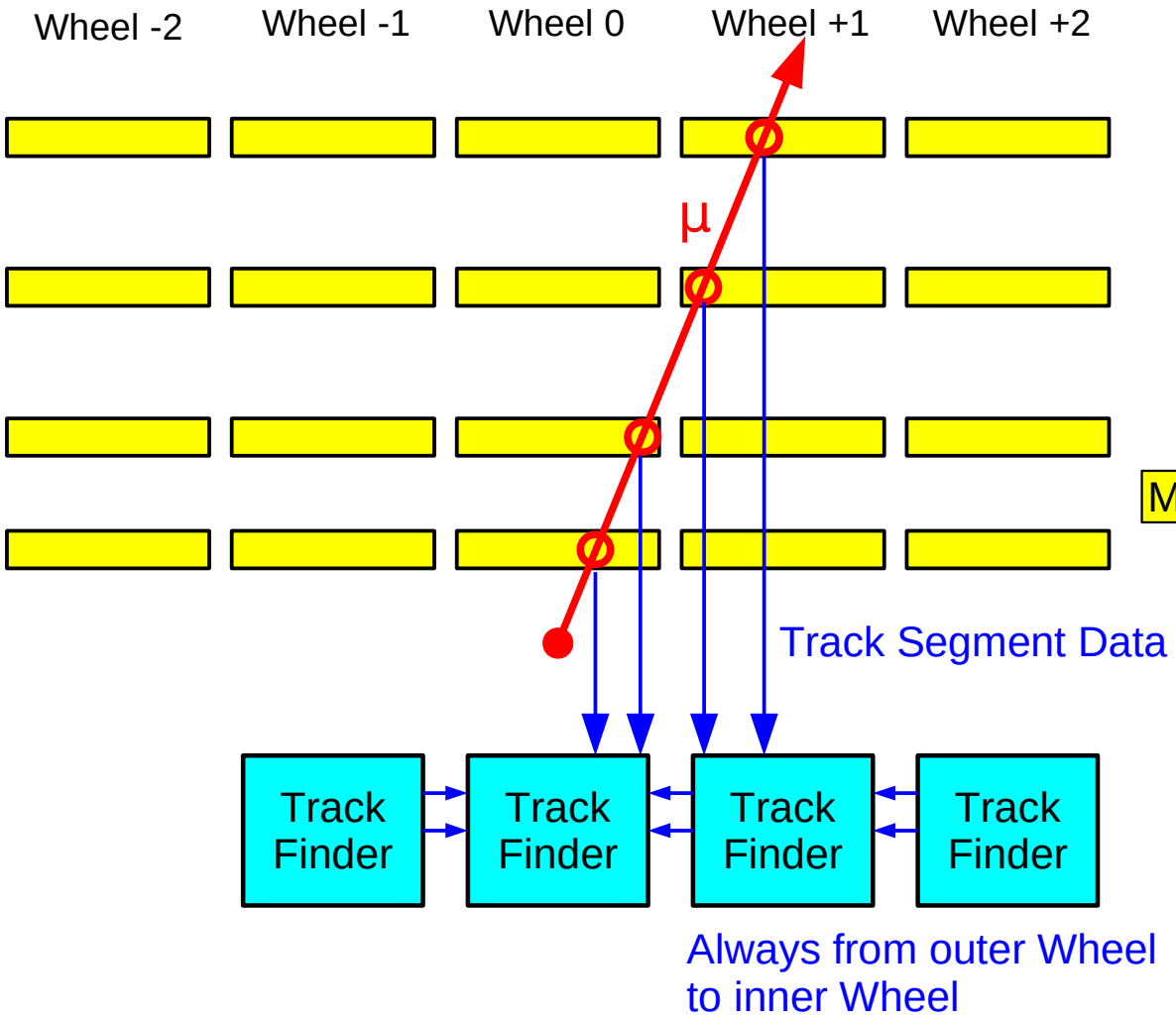
for Muons crossing Sector boundaries



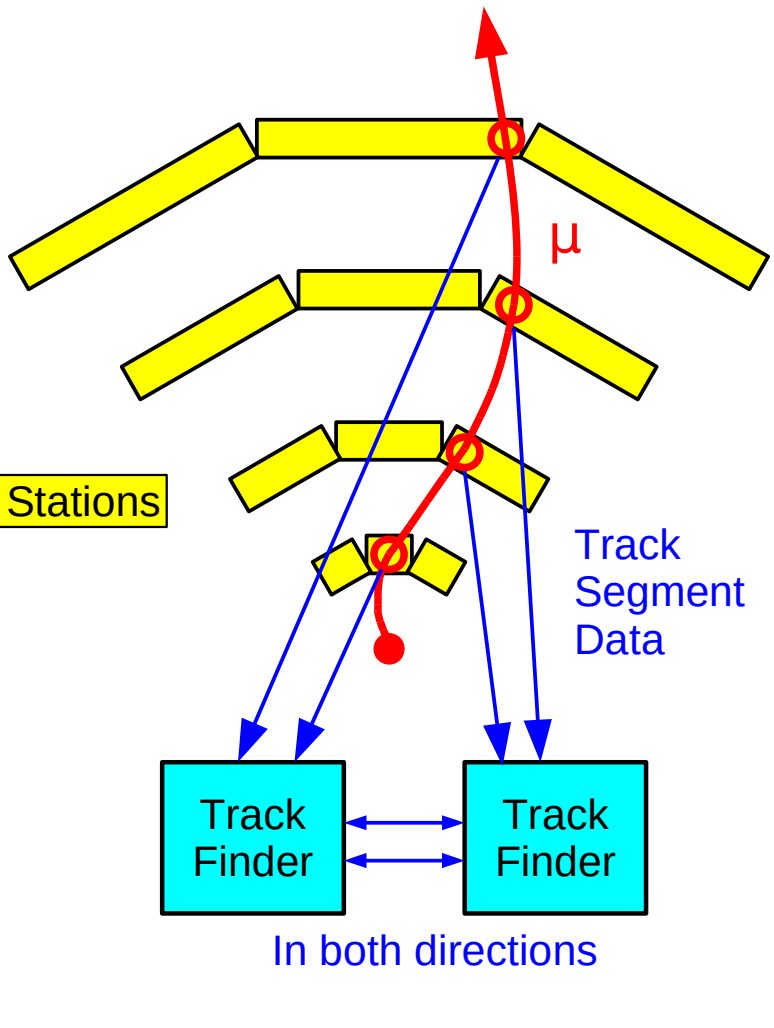
Eta View

Neighbour Connections

for Muons crossing Sector boundaries

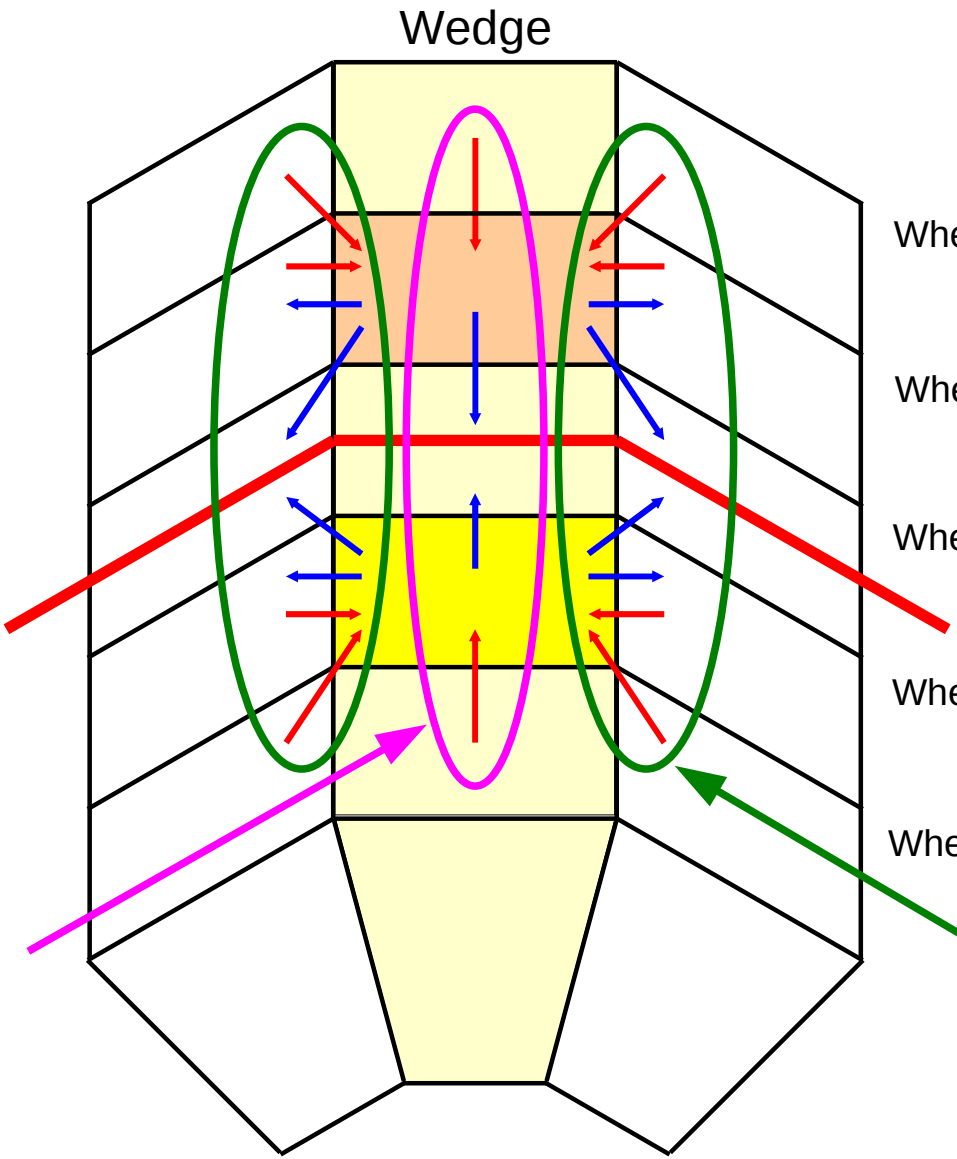


Eta View



Phi View

Neighbour Connections



To minimize L1 Latency all connections parallel !

No connections between positive and negative detector halves!

Data transfer inside Wedge GTL+ signals on the Backplane

Data transfer between Wedges multi-drop MLVD on flat cables “Green Salad”

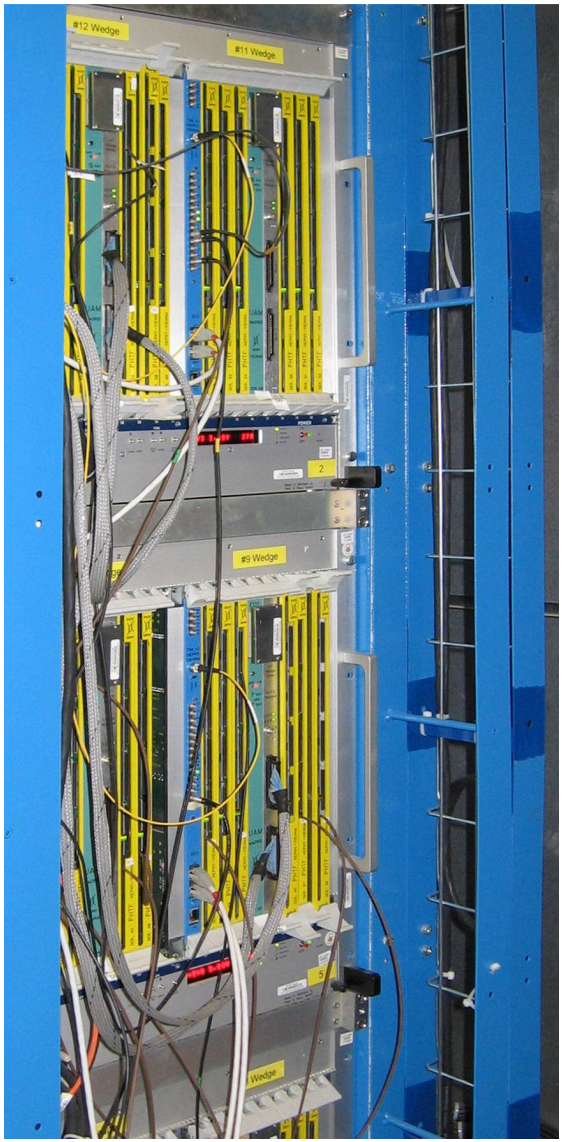
The “Green Salad”

Parallel Data Links
to decrease Latency

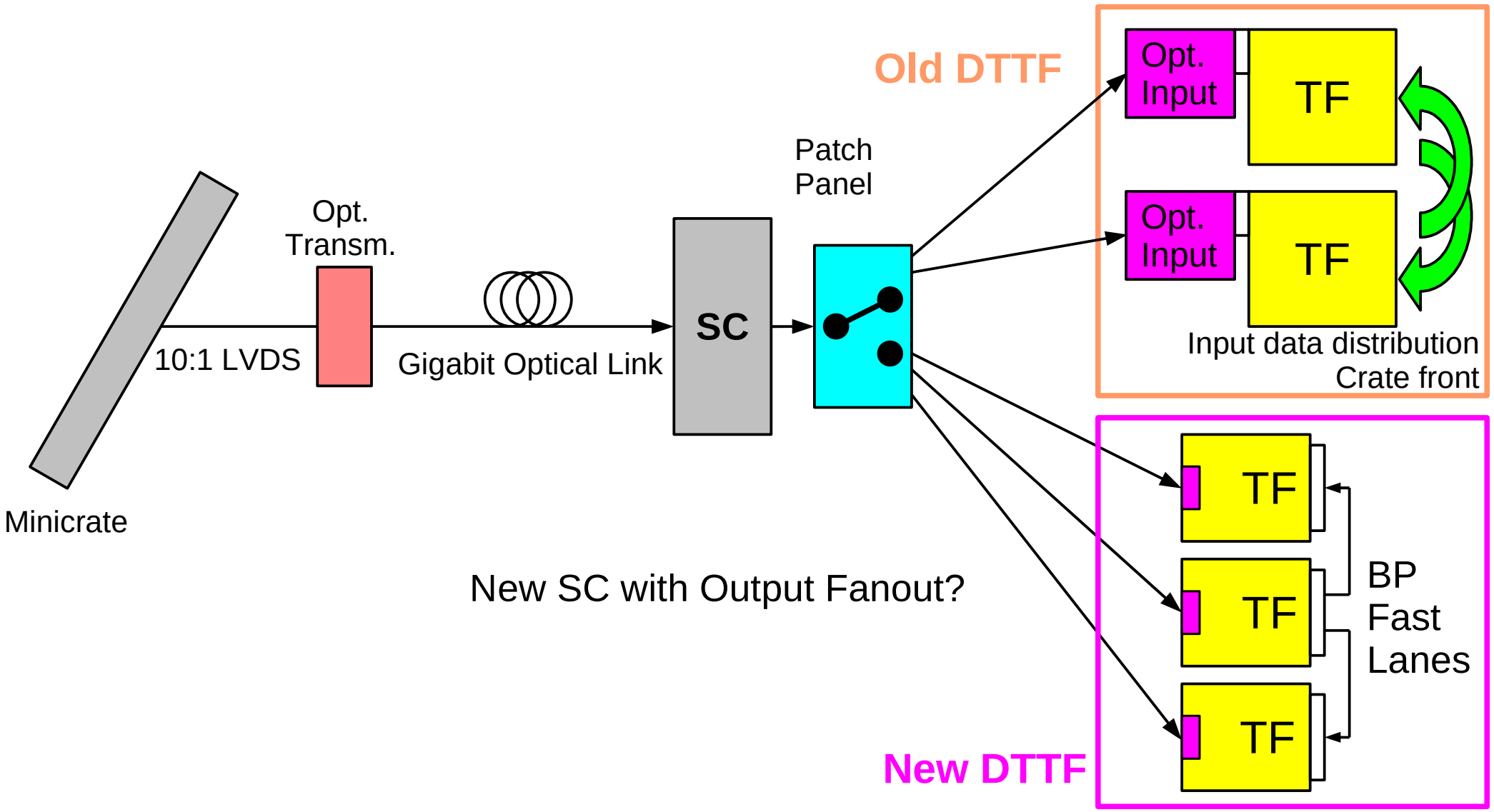
120 output connectors
7680 output pins
432 input connectors
27'648 input pins

A Maintenance Issue

The “Green Salad”



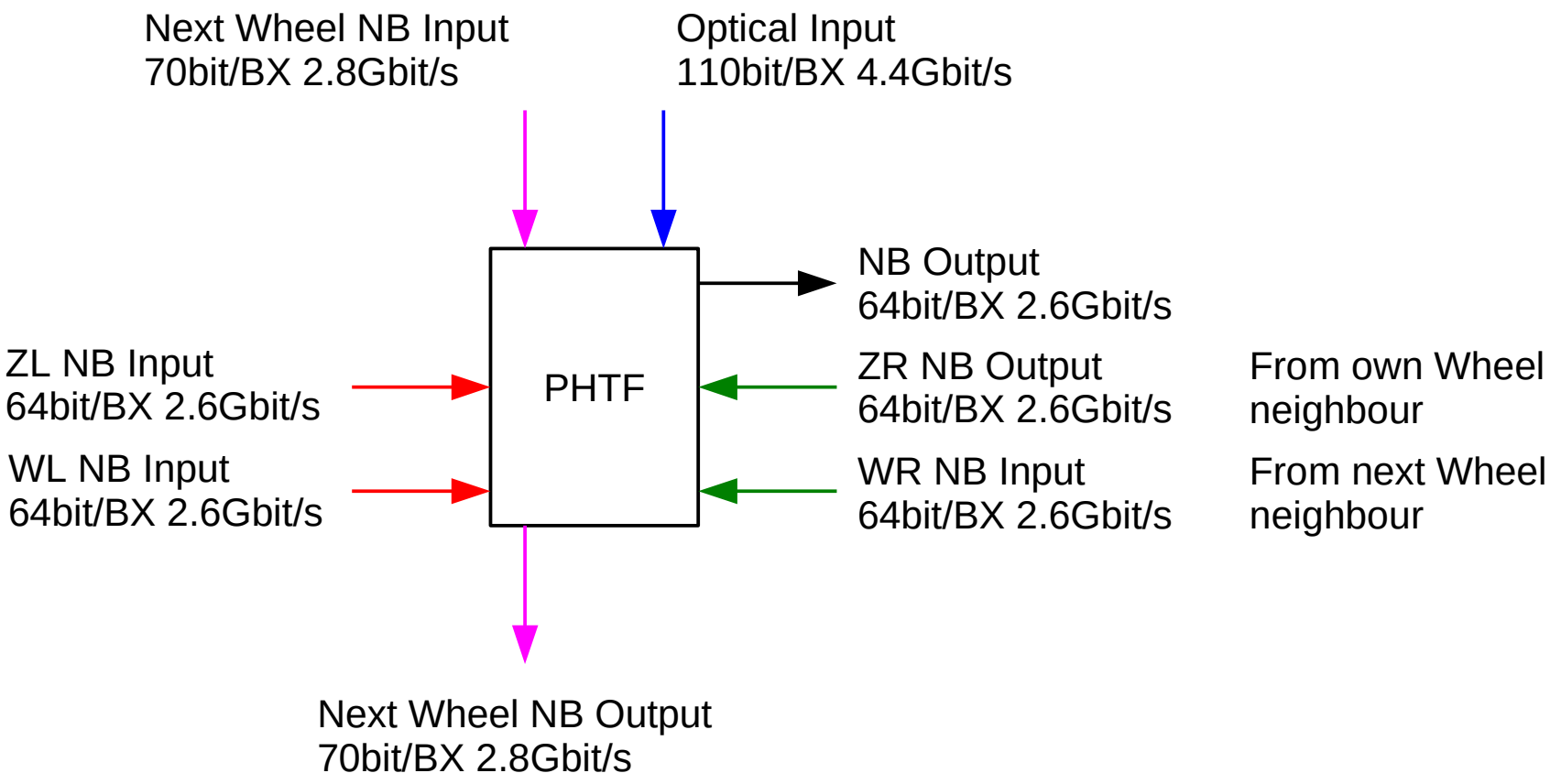
Trigger Object distribution on Backplane



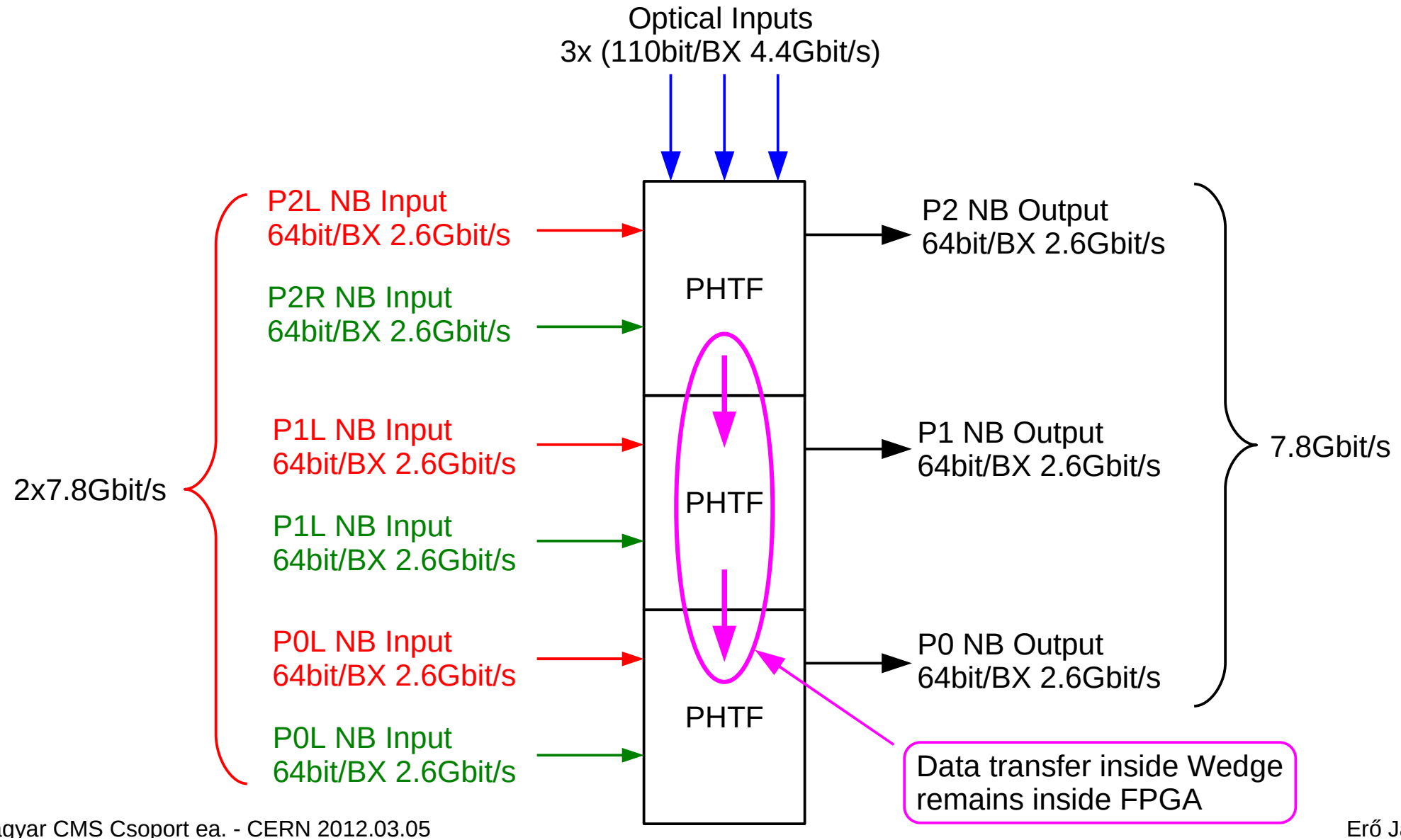
Baseline for Upgrade

- Technology goal: improve connections, reduce failure rate
- Put more logic into one Card (FPGA)
- Use Backplane connections instead of cables
- CMS: 12 DT Sectors – µTCA: 12 AMC Slots in one Crate
  - a half Wedge seems to be optimal Unit size
- Use CMS feature of independent Positive and Negative detector halves
  - Data from Wheel 0 must be shared between units serving Half Detectors
- Input data “as is”
  - new SC compatible with old one
- Use CERN background
  - central services and S/W development
    - DAQ, TTC can be of common design
    - control structure must be taken
- Smaller system costs less
  - 2 Crates, 24 TF Boards + Sorters

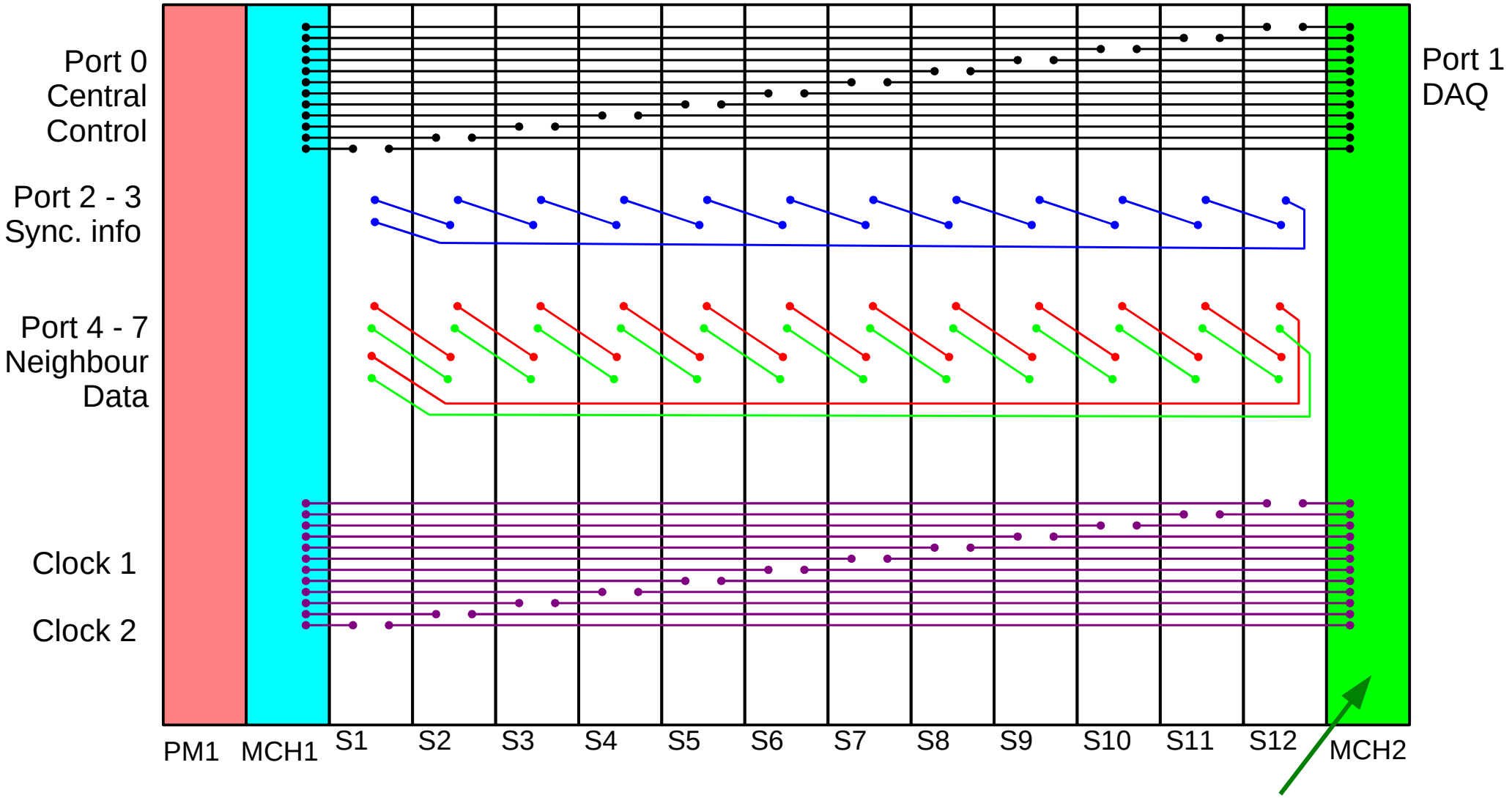
PHTF Sector I/O Bandwidth



I/O Bandwidth when Merging a half Wedge (0-1-2 Wheels) into one FPGA



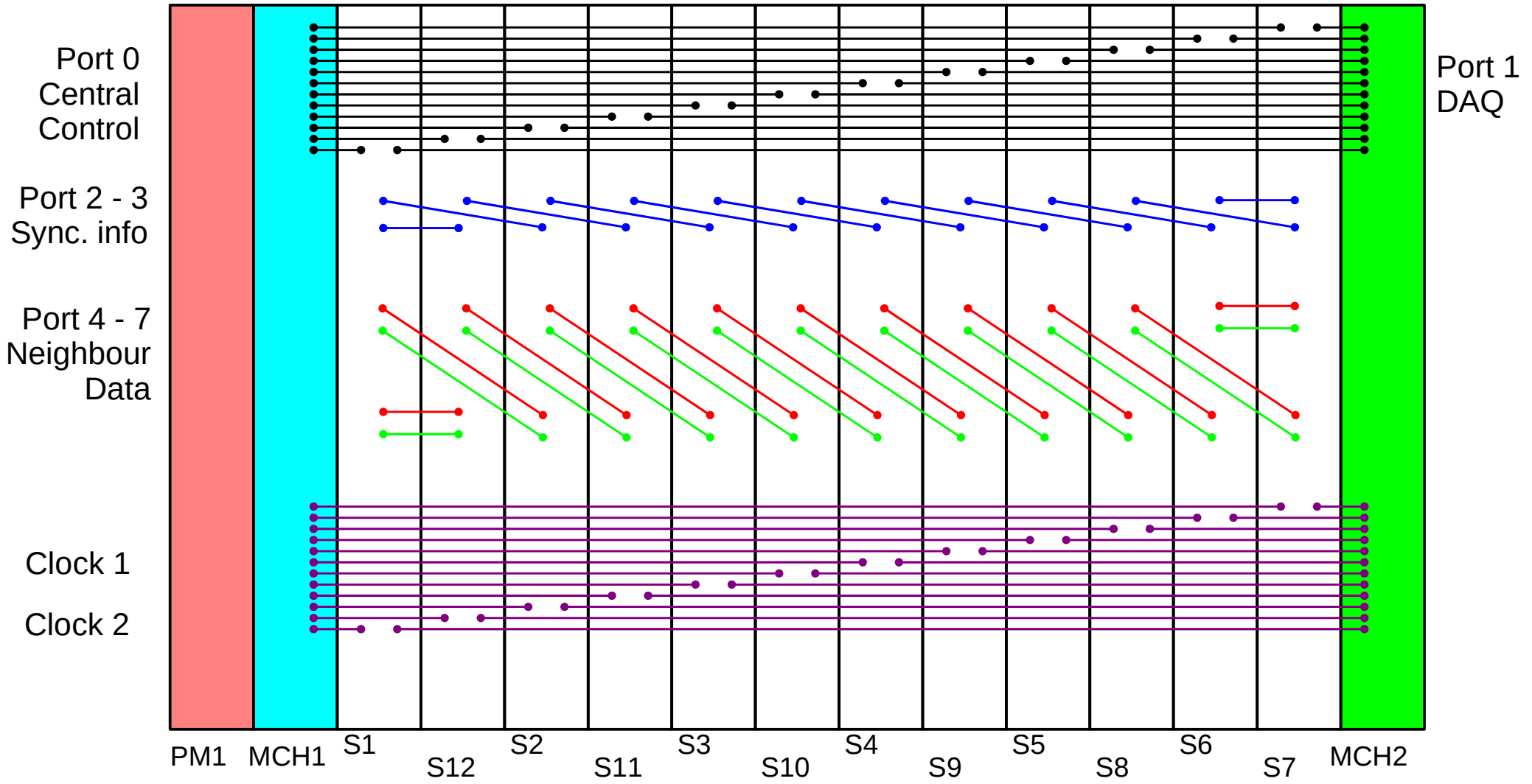
Custom µTCA Backplane for 12 Wheels



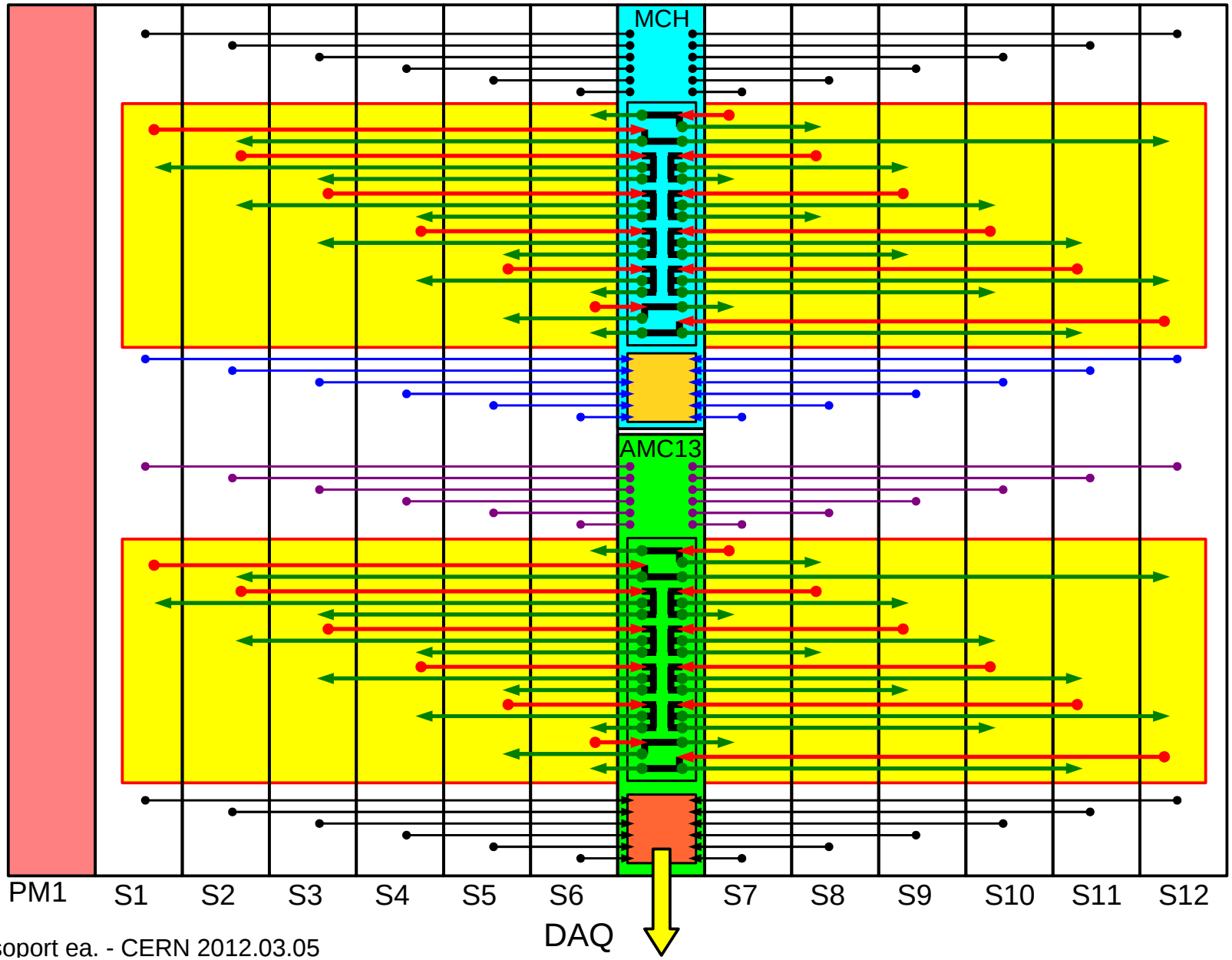
Special Board in place of MCH2: for DAQ and TTC control

Custom µTCA Backplane for 12 Wheels

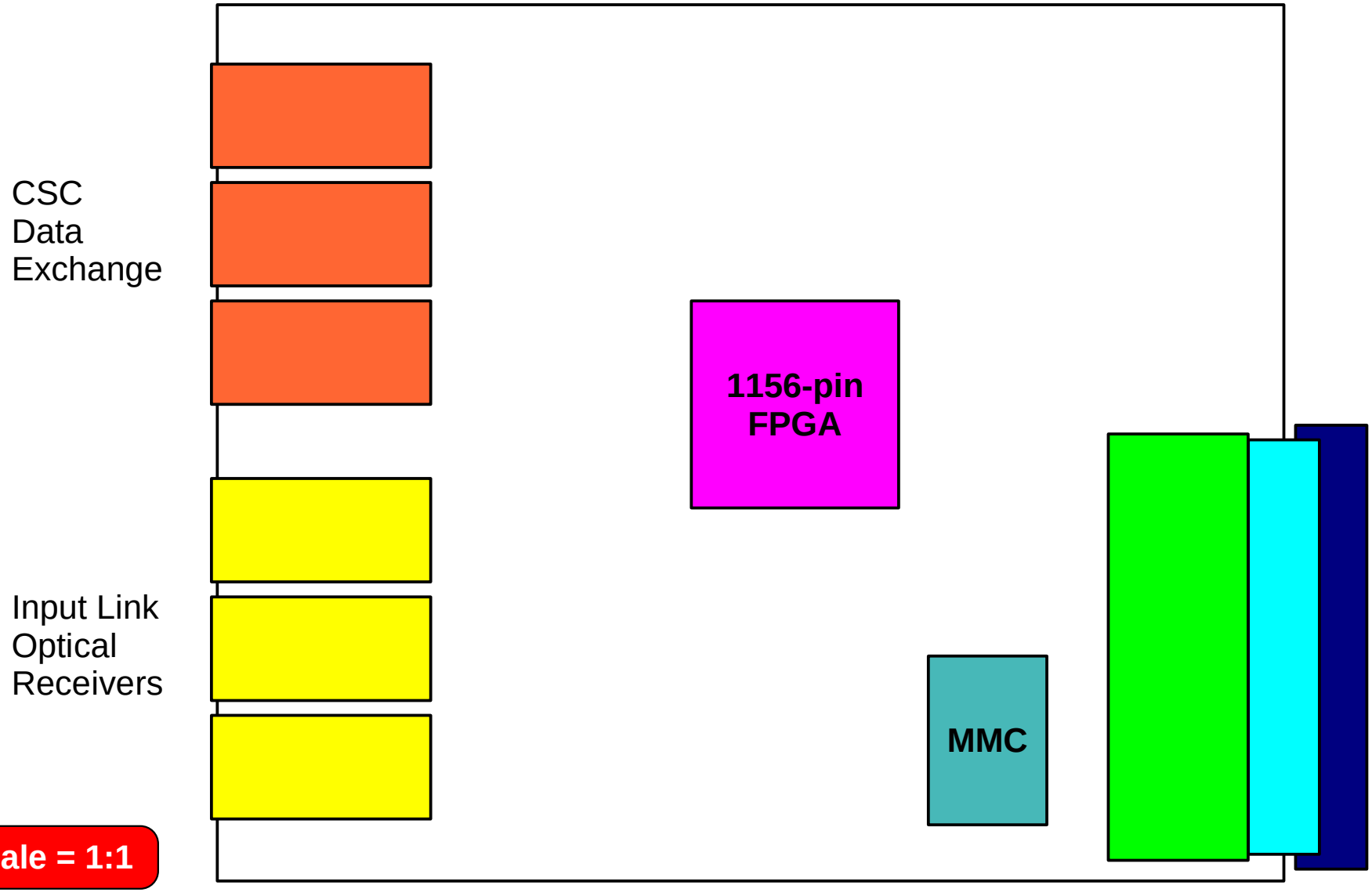
with all short Connections



With Standard Backplane (Vadatech VT891 opt.)

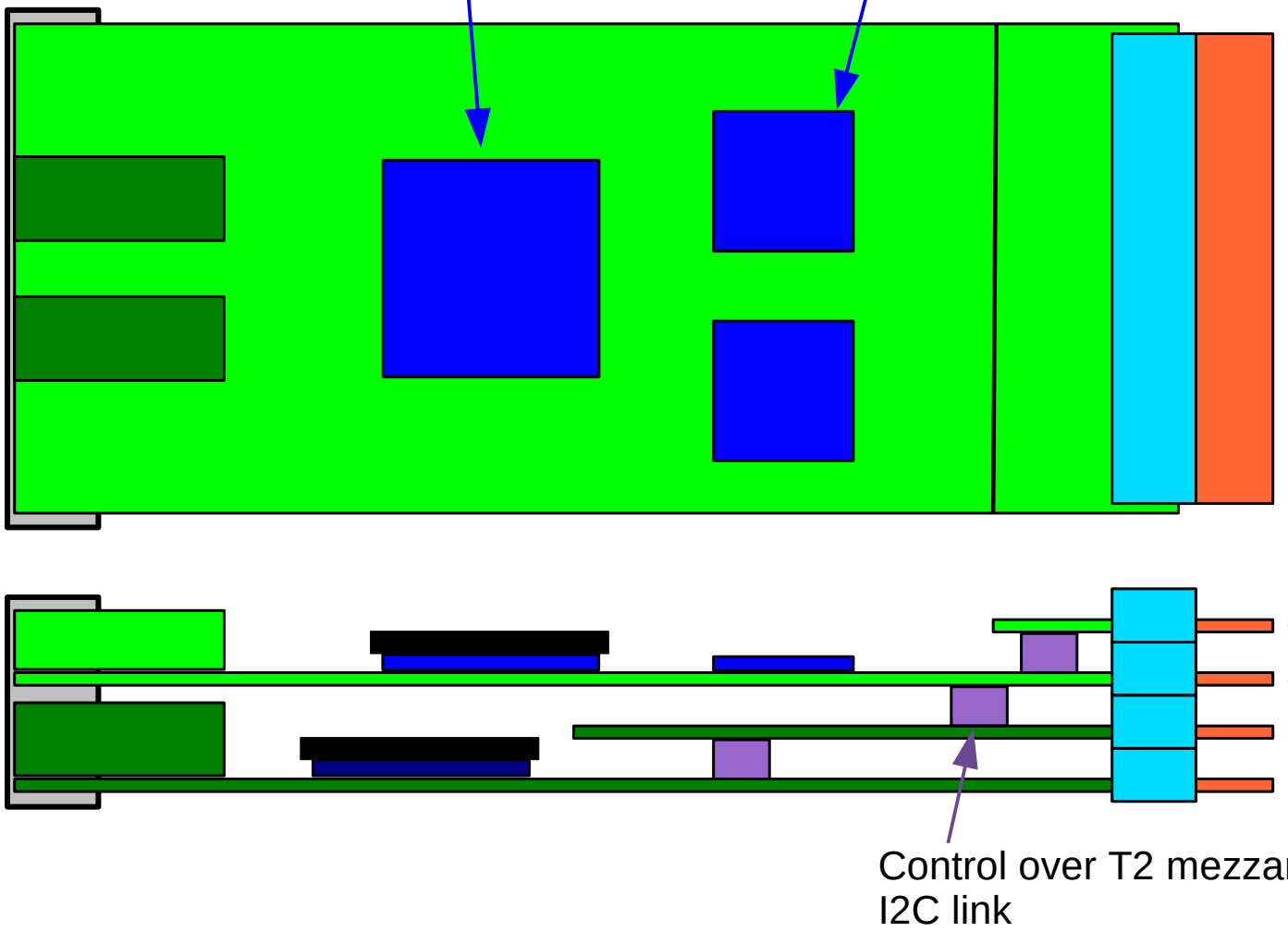


TF AMC Board Layout study



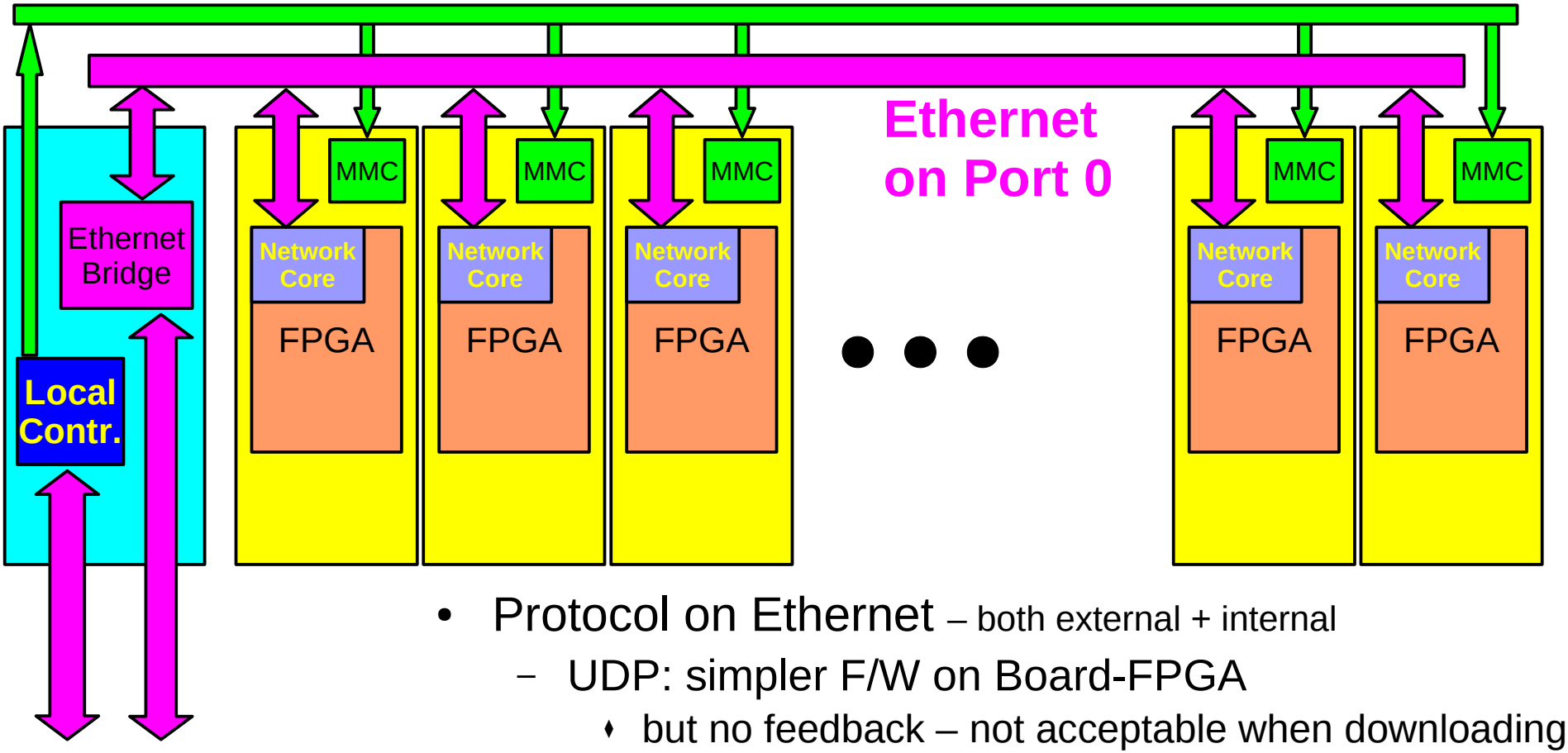
MMC: stand-alone block for “slow control”

Data Fanout as MCH/AMC13 mezzanine



µTCA Control Scheme

"Slow Control"

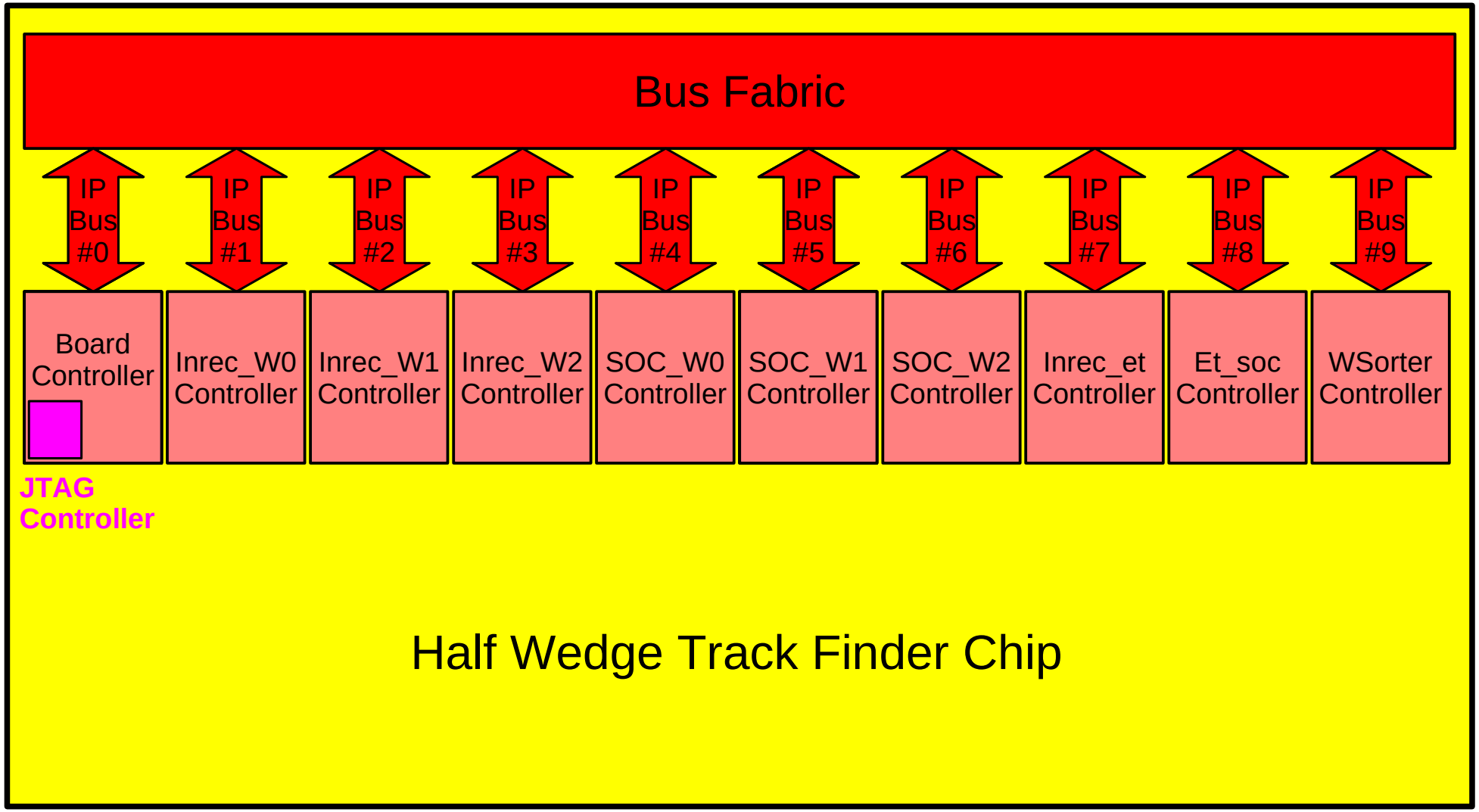


- Protocol on Ethernet – both external + internal
  - UDP: simpler F/W on Board-FPGA
    - but no feedback – not acceptable when downloading LUTs
  - TCP/IP
    - feedback built in – but processor (sequencer), memory needs
- PCIe on Port-0, not Ethernet

Goals for a new DTTF Control Scheme

- Design for merging 3 PHTFs and a half ETTF
- Keep present control structures
  - allows using existing Firmware VHDL blocks
  - simple merge scheme
  - small changes for maintenance programs and simulation data
  - easier application control programs
- Map control structures into **IPbus**
- IPbus is a F/W Core that maps VME-like structures into µTCA
  - uses UDP for simpler Firmware, less FPGA resources
  - CMS support
  - existing mapping scheme
  - use the same Entity for all control functions
    - synthesis optimizes parallel structures away

New Track Finder IPbus Structure



Back to the Physics Case

- Upgrade Main reason is Maintenance, but improvements for future physics
- Possible more output Trigger Muons
  - needs cooperation between Subsystems
  - Global Muon Trigger merge scheme changes
- Increase Output Muon parameter resolution
  - well, present system could also do – if GMT supports (present interface does not!)
- Refine TS parameter exchange in Overlap Region
- Present Charge assignment not really efficient
  - present system actually could improve, too

Feasibility Study, Prototyping

- Open Questions
  - Bandwidth Fitting
    - Trigger Object backplane distribution
    - CSC connection
    - Probably no troubles with:
      - DAQ Output
      - Trigger Output
      - Control
  - Optical Link Questions
    - Multi-Fiber Optical cables & connectors
      - Place and routing requirements
    - Patch Panel and/or Optical Splitting (Wheel 0) – new SC with fanout? when?
  - µTCA developments at CERN
    - Custom Backplane options – probably not necessary
    - DAQ output Options – DTTF can use this design
    - Control Options – implementation in progress
    - TTC Options – check AMC13
      - requirements are not very tight
      - discrepancy between Link clocking and LHC clock
        - problem for everybody at CMS